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EV 325214186 US

Single-chip Massively Parallel Analog-to-Digital Conversion

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CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of Application Serial No. 10/146,875, filed May 15, 2002, entitled "Single-chip Massively Parallel Analog-to-Digital Conversion" of the same inventors hereof, which application is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

[0002] The invention relates to analog-to-digital conversion circuits, and more particularly to a high speed analog-to-digital conversion circuit using a massively parallel analog-to-digital conversion technique.

DESCRIPTION OF THE RELATED ART

[0003] Analog-to-digital conversion (ADC) is performed to convert an analog signal to a digital number indicative of the amplitude of the analog signal. The digital number is typically a digital code in 4-bit to 10-bit depending on the precision of the conversion. Analog-to-digital conversion is performed by sampling the analog signal at a predetermined frequency and converting the amplitude of the sampled signal to a digital number representative of the amplitude. The speeds of the analog-to-digital conversion typically range from 15 to 300 megasamples per second (MSPS). To accurately represent an analog signal in digital form, the analog signal must be sampled at at

least twice the highest frequency present in the analog signal. Therefore, for a high frequency signal, such as a 200 MHz analog signal, the speed of the ADC conversion must be at least 400 MSPS to provide an accurate representation.

[0004] Analog-to-digital conversion is commonly used in applications such as audio signal processing, video and medical imaging and high speed communications. The analog signals are converted to digital representations so that subsequent digital signal processing (DSP) techniques can be applied to the digital data. DSP techniques for processing digital data can include data compression, noise filtering, data storage, noiseless transmission of data, and digital encryption of data.

[0005] For applications operating at very high frequency or very high transmission rate, a high speed (e.g. 400 MSPS) analog-to-digital (A/D) converter is needed to ensure accurate conversion. Such high speed A/D converters are typically very complex and complicated to design. A single-chip high speed A/D converter can be quite large and can consume large amount of power in operation. It is desirable to provide a high speed A/D converter that is smaller and simple to design so that power consumption and manufacturing cost can be reduced.

SUMMARY OF THE INVENTION

[0006] In accordance with one embodiment of the present invention, a circuit includes an input terminal coupled to receive an analog input signal, a multiple number of sample-and-hold circuits and a multiple number of analog-to-digital (A/D) converters. The input terminal of each of the sample-and-hold circuits is coupled to the input terminal of the circuit

receiving the analog input signal. Each of the A/D converters has an input terminal and an output terminal, where the input terminal is coupled to an output terminal of a corresponding one of the sample-and-hold circuits. In operation, the sample-and-hold circuits sample the analog input signal sequentially and store a multiple number of analog samples at each of the sample-and-hold circuits. The A/D converters convert the analog samples in parallel to generate digital values at the output terminals of each of the A/D converters representative of the analog samples.

[0007] In one embodiment, the A/D converters are implemented based on a multi-channel bit-serial (MCBS) analog-to-digital conversion scheme. Each A/D converter includes a comparator receiving a first signal having a number of levels and a latch receiving and a series of binary signals. The A/D converter operates to convert the analog sample to a digital code representation.

[0008] The present invention is better understood upon consideration of the detailed description below and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 is a schematic diagram of an A/D converter according to one embodiment of the present invention.

[0010] Figure 2 is a diagram illustrating a representative analog input signal and the operation of the A/D converter of the present invention.

[0011] Figure 3 is a schematic diagram illustrating the basic architecture of the MCBS ADC technique.

[0012] Figure 4 is a schematic diagram illustrating an A/D converter including a two-dimensional array of A/D converter elements according to one embodiment of the present invention.

[0013] Figure 5 is a timing diagram illustrating the row access signal and column access signal for controlling the A/D converter of Figure 4 according to one embodiment of the present invention.

[0014] Figure 6 is a schematic diagram illustrating an A/D converter according to another embodiment of the present invention.

[0015] Figure 7 is a schematic diagram illustrating an A/D converter including a two-dimensional array of A/D converter elements according to an alternate embodiment of the present invention.

[0016] Figure 8 is a schematic diagram illustrating an A/D converter including a two-dimensional array of A/D converter elements according to an alternate embodiment of the present invention.

[0017] Figure 9 is a schematic diagram illustrating an A/D converter including a two-dimensional array of A/D converter elements according to an alternate embodiment of the present invention.

[0018] In the present disclosure, like objects which appear in more than one figure are provided with like reference numerals.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019] In accordance with the principles of the present invention, an analog-to-digital (A/D) converter includes multiple A/D converter elements configured to perform analog-to-digital conversion of an analog signal in a massively parallel fashion. In one embodiment, the A/D converter elements are low-speed A/D converters having a conversion rate of about 50 MSPS or less. The A/D converter of the present invention can achieve high speed conversion by performing multiple conversions in parallel using low-speed A/D converters. Because low-speed A/D converters are simpler to implement and because control circuitry can be shared among the multiple A/D converter elements, the A/D converter of the present invention can be made smaller in size and with fewer transistors than conventional high speed A/D converters. Accordingly, the A/D converter of the present invention consumes less power and reduces the manufacturing cost. Furthermore, the use of multiple low-speed A/D converters reduces the design complexity of the A/D converter so that single-chip high speed A/D converters in different configurations can be readily constructed in accordance with the principles of the present invention.

[0020] Figure 1 is a schematic diagram of an A/D converter according to one embodiment of the present invention. Referring to Figure 1, A/D converter 100 includes an array of sample-and-hold circuits 104a to 104c and an array of A/D converter elements 106a to 106c. An output terminal of each sample-and-hold circuit is coupled to the input terminal of a corresponding A/D converter element. In the present embodiment, each of sample-and-hold circuits 104a to 104c includes a switch (S1-S3) and a capacitor

C_{SH}. A/D converter 100 includes one input channel 102 for receiving an analog signal and generates a digital output on output bus 110. In the present embodiment, A/D converter 100 provides digital data representing the analog input signal in a bit-serial format. In other embodiments, A/D converter 100 can provide the digital data in a parallel format where the databits are provided on output bus 110 simultaneously. Typically, A/D converter 100 is fabricated as a single integrated circuit having an input pin receiving the analog input signal and an output pin or an output bus providing the digital output.

[0021] Sample-and-hold circuits 104a to 104c operate in a conventional manner under the control of a select signal. In the present embodiment, the select signal causes switches S1 to S3 to close sequentially so that the analog input signal is sampled at three consecutive sampling times. At each of the sampling time, the amplitude of the analog input signal is stored on the respective capacitor C_{SH}. After the analog input signal have been sampled by sample-and-hold circuits 104a to 104c, A/D converter elements 106a to 106c operate to convert each sample in parallel to generate a digital output indicative of the amplitude of the sampled analog signal. In the present embodiment, the output terminals of A/D converter elements 106a-106c are coupled to an array of output latches 108 which operates to transfer the digital output signals from each of A/D converter elements 106a to 106c onto output bus 110.

[0022] Each of A/D converter elements 106a to 106c can be constructed as a low-speed A/D converter. Because the analog input signal in input channel 102 is being sampled and digitally converted in parallel at three sampling times by A/D converter

elements 106a to 106c, A/D converter 100 can achieve an effective conversion rate that is three times the conversion rate of each of the converter element. For example, A/D converter elements 106a to 106c can each have a conversion rate of only 20 MSPS. A/D converter 100 will have an effective conversion rate of 60 MSPS. By providing a large number of A/D converter elements to convert the analog input signal in parallel, A/D converter 100 can realize a very high conversion rate. In the present illustration, A/D converter 100 includes only three A/D converter elements. In other embodiments, A/D converter 100 may include a large number of converter elements to realize a high A/D conversion rate.

[0023] Figure 2 is a diagram illustrating a representative analog input signal and the operation of the A/D converter of the present invention. Referring to Figure 2, an analog signal 120 is being converted by A/D converter 100 of Figure 1. At the start of the analog to digital conversion process, the analog input signal 120 is sampled by sample-and-hold circuit 104a to 104c in sequence. Then A/D converter elements 106a to 106c operate to convert the analog samples to digital output. Then, the process repeats where analog input signal 120 is sampled again and digitally converted again by A/D converter 100. In the present illustration, even though each A/D converter element has a conversion rate of only 1000 samples per second, the effective conversion rate for A/D converter 100 is 3000 samples per second as analog input signal 120 is continuously being sampled and converted in parallel by sample-and-hold circuits 104a to 104c and A/D converter elements 106a to 106c.

[0024] As described above, A/D converter elements 106a to 106c can be constructed as any low-speed ADC converters. For instance, an A/D converter having a conversion rate of less than about 50 MSPS can be used. Low-speed ADC converters are preferred in the A/D converter of the present invention because low-speed A/D converters tend to be smaller and less complicated to design and implement. In accordance with one embodiment of the present invention, the A/D converter elements are constructed based on a multi-channel bit-serial (MCBS) analog-to-digital conversion scheme. MCBS analog-to-digital conversion is described in U.S. Patent No. 5,801,657 of Fowler et al. ("the '657 patent"). The MCBS ADC scheme described in the '657 patent can significantly improve the overall system performance while minimizing the size of the A/D converters. The '657 patent is incorporated herein by reference in its entirety.

[0025] Figure 3 replicates Figure 1A of the '657 patent and illustrates the basic architecture of the MCBS ADC technique. In Figure 3, A/D converter 14 includes a multiple number of conversion channels, such as Channel 0 to Channel N, where each conversion channel is associated with an analog input signal In0 to InN. Each conversion channel contains a 1-bit comparator 16a-n and a 1-bit latch 17a-n. Comparators 16a-n and latches 17a-n are controlled by external control signals RAMP and BITX. The two control signals are generated by a micro-controller 18 and a digital-to-analog (D/A) converter 19 and are broadcasted to all conversion channels, i.e., Channel 0 to Channel N.

[0026] The MCBS ADC scheme of the '657 patent provides several advantages. First, because all conversion channels are operated simultaneously, maximum throughput can be achieved. Second,

because each conversion channel uses simple circuitry, i.e. each input channel includes only one 1-bit comparator and one 1-bit latch, the A/D converter consumes minimum circuit area in implementation. Furthermore, because the more complicated control circuitry, such as micro-controller 18, are shared among all conversion channels, the overhead of the control circuitry is spread among all of the conversion channels. These advantages make MCBS A/D converter suitable for use in digitizing systems for converting a very large number of analog signals in parallel.

[0027] In accordance with the present invention, instead of applying the multi-channel bit-serial (MCBS) analog-to-digital conversion technique to the conversion of a very large number of analog signals simultaneously, the MCBS ADC technique is applied to the conversion of one or a few analog signals for realizing a very fast conversion rate. In one embodiment of A/D converter 100, each A/D converter element is implemented as one conversion channel of the MCBS A/D converter. The control circuitry, such as the microcontroller and the DAC, is shared among all the A/D converter elements. Because each conversion channel of an MCBS A/D converter can be made very small (22 transistors per converter on the average), the A/D converter of the present invention can be constructed on a single integrated circuit ("a chip") even when the A/D converter has a very large number of A/D converter elements.

[0028] Figure 4 is a schematic diagram illustrating an A/D converter including a two-dimensional array of A/D converter elements according to one embodiment of the present invention. Referring to Figure 4, A/D converter 200 includes a two-dimensional array of ADC cells 212. Each ADC cell includes a

sample-and-hold circuit coupled to an A/D converter element. Specifically, in each ADC cell, an output terminal of a sample-and-hold circuit is coupled to an input terminal of an A/D converter element. Each ADC cell 212 operates to sample the analog input signal and covert the analog sample to a digital output. In the present embodiment, A/D converter 200 includes only one input channel, receiving an analog input signal Input0, and provides a digital output, Output0, on an output bus 210.

[0029] The number of ADC cells in A/D converter 200 of the present invention can vary depending on the application the A/D converter is used. However, because each A/D converter element is small in size, A/D converter 200 can include up to millions of ADC cells to achieve a very high conversion rate. Because the sample-and-hold circuit typically operates at a much faster speed than an A/D converter, the A/D converter of the present invention is able to sample and hold a large number of samples of an analog signal for parallel conversion using the array of A/D converter elements. In this manner, very high speed analog-to-digital conversion can be achieved even when the individual A/D converter element has a low conversion rate. In the present embodiment, A/D converter 200 includes an array of one million ADC cells. Each A/D converter element can operate at a rate of 1000 conversions per second. Therefore, A/D converter 200 can realize an aggregate conversion rate of 1000 × 1 million = 1 billion conversions per second.

[0030] As described above, because each A/D converter element can be constructed as a low-speed A/D converters and is thus small in size, the entire array of ADC cells can be fabricated on a single integrated circuit. In the present embodiment, A/D

converter elements in A/D converter 200 are constructed based on the MCBS ADC technique. Thus, each A/D converter element is implemented as one conversion channel of the MCBS A/D converter. Because each conversion channel can be implemented using very few transistors (e.g. 5.5 transistors on average), A/D converter 200 can be manufactured as a single chip high speed analog-to-digital conversion circuit including at least 1 million A/D converter elements.

[0031] In operation, analog input signal Input0 is provided to A/D converter 200. The analog input signal is sequentially sampled by each of the sample-and-hold circuits until a sample of the analog input signal is loaded into each of the ADC cells 212. Then A/D converter 200 activates the A/D converter elements in each of the ADC cells to perform massively parallel analog-to-digital conversion of the sampled signals. A/D converter 200 includes a readout circuit 218 for reading out the digital output from each of the A/D converter elements sequentially. In the present embodiment, the digital output is provided on output bus 210 as Output0 in serial format. Alternately, the digital output can be provided on output bus 210 in parallel format.

[0032] In the present embodiment, the array of ADC cells is addressed using a column access and row access addressing scheme commonly used in random access memory (RAM) circuits. The use of a conventional memory accessing scheme has the advantage of allowing a large number of cells to be loaded without degrading the analog input signal. The column access signal and the row access signal operate to ensure that each ADC cell samples the analog input signal sequentially in a predetermined order so that a very high speed analog-to-digital conversion can be realized.

A/D converter 200 may include other supporting circuitry to facilitate the loading of the ADC cells and the reading of the converted signals from each A/D cell. For example, a column refresh circuit 219 may be included to precharge the bitlines (the output signal lines) coupled to the output terminals of the A/D cells. The operation of the column refresh circuit to refresh bitlines and facilitate readout of signals in a memory array is well known in the art of memory design.

[0033] Figure 5 is a timing diagram illustrating the waveform of the row access signals and column access signals for controlling A/D converter 200 according to one embodiment of the present invention. Referring to Figure 5, the row access signal S_r0, controlling the first row of ADC cells, is first activated to enable the first row of ADC cells to sample the analog input signal. Then, the column access signals S_c0, S_c1, S_c2, and S_c3 are activated sequentially so that each of the ADC cells in the first row of A/D converter 200 samples the analog input signal at a different but sequential time interval. After the first row of ADC cells has sampled the analog input signal, row access signal S_r0 is deactivated and row access signal S_r1, controlling the second row of ADC cells, is activated. The column access signals S_c0, S_c1, S_c2, and S_c3 are again activated sequentially to enable the ADC cells in the second row of A/D converter 200 to sample the analog input signal. The operation of the row access signals and column access signals allows the entire array of ADC cells to sequentially sample the analog input signal so that analog-to-digital conversion can be carried out in a massively parallel manner.

[0034] According to one embodiment of the present invention (illustrated in Figure 8), the array of ADC cells in A/D converter 200 may be divided into two banks to facilitate readout of the digital output from the A/D converter elements. Thus, in operation, digital output can be read out from the first bank of ADC cells while the second bank of the ADC cells is sampling and converting the analog input signal, and vice versa. In this manner, the speed of the analog-to-digital conversion is increased because the ADC converter alternates between the two banks of ADC cells so that one bank of ADC cells is always generating digital output.

[0035] In an alternate embodiment (illustrated in Figure 9), each ADC cell 212 of A/D converter 200 may further include a second sample-and-hold circuit coupled in parallel to the first sample-and-hold circuit. The two sample-and-hold circuits operate in concert to eliminate dead time during which the A/D converter elements wait for the next set of samples to be processed. In operation, the first sample-and-hold circuit in each of the ADC cells samples the analog input signal and provides the first analog sample to the A/D converter element. While the A/D converter element is converting the first analog sample, the second sample-and-hold circuit in each of the ADC cells samples the analog input signal to collect a second analog sample. When the A/D converter element has completed the conversion of the first analog sample, the A/D converter element can immediately proceed to convert the second analog sample stored at the second sample-and-hold circuit. In this manner, the A/D converter element can be operated continuously to convert analog samples stored in each of the first and second sample-and-hold circuits.

[0036] Figure 6 is a schematic diagram illustrating an A/D converter according to another embodiment of the present invention. Like elements in Figures 4 and 6 are given like reference numerals to simplify the discussion. Referring to Figure 6, A/D converter 300 includes a two dimensional array of ADC cells 212 and readout circuit 218 for sampling and converting analog signals in a massively parallel fashion. A/D converter 300 is different from A/D converter 200 in that A/D converter 300 includes multiple input channels. In the present embodiment, A/D converter 300 includes five input channels, Input0 to Input4, for receiving five analog input signals. A multiplexer 220, such as a programmable multiplexer, is used to select the different input channels for coupling to the array of ADC cells.

[0037] In one embodiment, multiplexer 200 operates to select one input channel to be processed by the entire array of ADC cells. For each input channel, a very high conversion rate can be realized. In another embodiment, the array of ADC cells is divided into banks where each bank of ADC cells is associated with one input channel. In this manner, each input channel is provided with dedicated analog-to-digital conversion capability. Although the conversion rate for each channel is reduced when the A/D converter includes dedicated banks of ADC cells, the conversion rate for each input channel can still be very high as long as sufficient number of A/D converter elements is included in each bank. For instance, when A/D converter 300 includes 100 input channels and 1 million ADC cells, each A/D converter element having a conversion rate of 1000 conversions per second, A/D converter 300 can still realize 10 millions conversions per input channel per second. The improvement in conversion rate in

a multi-channel A/D converter of the present invention is still significantly increased from conventional A/D converters.

[0038] According to another embodiment of the present invention (illustrated in Figure 7), an analog shift register can be used in place of the sample-and-hold circuit in each of the ADC cells of the A/D converter of the present invention. Referring to Figure 7, an array of analog shift registers 240 can be used to load samples of the analog input signal sequentially into each ADC cell. The array of ADC cells can then perform analog-to-digital conversion in a massively parallel fashion. The analog shift registers must operate fast enough to ensure that the array of ADC cells can be loaded in a time shorter than the conversion time of the A/D converter element. The speed of the analog shift registers may limit the number of ADC cells that can be integrated in an A/D converter of the present invention. Alternately, signal buffering or boosting can be included to recover the signal integrity and to speed up the shifting operation so that analog shift registers can be applied in a large array of ADC cells.

[0039] The A/D converter of the present invention has numerous applications where high speed analog-to-digital conversion is performed. For instance, the A/D converter of the present invention can be used in digital televisions for converting analog video signals, in satellite TV decoders, in digital video recorders, in digital oscilloscopes and in digital network switches.

[0040] The above detailed descriptions are provided to illustrate specific embodiments of the present invention and are not intended to be limiting. Numerous modifications and

variations within the scope of the present invention are possible. The present invention is defined by the appended claims.